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主　論　文　の　要　旨

論文題目　METHODOLOGY AND A FRAMEWORK FOR EFFICIENT DESIGN SPACE EXPLORATION AT A SYSTEM LEVEL
（システムレベル設計における効率的な設計空間探索のための手法およびフレームワーク）

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論　文　内　容　の　要　旨

This dissertation presents a system-level design framework for design space exploration of embedded systems.

Design space of embedded systems has been growing. Recent embedded systems have been required to have multiple functionalities in themselves. In order to realize the functionalities under their constraints such as performance, hardware areas and power consumptions, they have been adopting complex architecture which have not only dedicated hardware modules but also multiple processors. Since the performance and costs of embedded systems depend on the mapping of their functionalities onto hardware modules and processors, system designers should find an appropriate mapping efficiently from the large design space.

System-level design is one of key methodologies in order to deal with the large design space. The main purpose of system-level design is to find appropriate architecture of systems including hardware architecture such as the number of processors and dedicated hardware and mapping of functionalities onto them.

In system-level design, system designers generally develop models of systems at high level and evaluate mappings of them. If the evaluation results are not sufficient for their requirements, designers change the mapping or refine the models, and evaluate them again. The designers iterate refinement and evaluation until the models meet their requirements.

Our framework consists of four tools which cover overall system-level design: SystemBuilder-MP, covalidation environment, system-level profilers and a fast performance estimation tool. The main objective of our framework is to sup-

port the design space exploration by iteration of modeling, implementation and evaluation.

Modeling was done in the system description model defined by SystemBuilder-MP. Models are automatically converted into implementations according to a mapping by SystemBuilder-MP. With the SystemBuilder-MP, system designers can obtain implementations of a system without manual works and thus can easily evaluate them. The functionality of the implementations can be validated in short time by the covalidation environment which utilizes a fast Real-Time OS model and an FPGA. Mappings of a system are evaluated by executing the implementations on an FPGA (Field Programmable Gate Array). The system-level profilers are automatically instrumented into the implementations on an FPGA by SystemBuilder-MP and records behavior of them. With visualization of profiles recorded by the profilers, system designers can easily analyze their performance such as parallelism in order to refine them. Moreover, the fast performance estimation tool estimates performance of various mappings fast and accurately from profiles obtained by a few implementations. Using the performance estimation tool, system designers can prune mappings which are obviously unnecessary without implementations of them.

With these tools, designers can explore mappings of a system fast and easily since most of works for implementation and evaluation are done automatically. Therefore efficient design space exploration at a system-level is realized.

This dissertation describes the detail of above tools and evaluates them using some case studies. With the case studies, the smoothness and easiness of design space exploration at a system level are demonstrated.